ISSN: 2277-9655
Impact Factor: 1.852

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Analysis of Vector Modulation in Three-Phase Z-Source Inverters

Mr.T.Yuvaraja[*1], Dr. M.Gopinath[2]

[*1]Research Scholar, Department of EEE, Meenakshi Academy of Higher Education and Research, (MAHER UNIVERSITY), Chennai, India

[2]Professor, Department of EEE,Dr.N.G.P. Institute of Technology, Coimbatore, India

yuvarajastr@gmail.com

Abstract

The performance and behavior of vector modulation in three phase Z source inverters is proposed under difference switching controls and their maximum voltage stress across the voltage gain. The efficiency in terms with duty ratio is analyzed. Space vector modulation is the newly excited method for all renewable energy sources are in need of multilevel power electronics in form of multilevel inverters. The mind behind the pulses created by the inverters is the SVPWM. This modulation type is implemented as a major proposed model. This vector model to locate and create the desired sinusoidal-shaped waveform under six parts of shoot through time intervals and it will reduce the inductor current ripples and improve Three phase ZSI efficiency. Simulation results of the prototyped are been obtained and analyzed.

Keywords: Power conversion, space vector modulation, Z source/ quasi-Z-source inverters.

Introduction

Every proposed work which deals with renewable energy is in need of renewable energy conversion in form of multilevel power electronics. This thesis approaches three-level converters in a wave power conversion point of view and covers the calculation and implementation of a pulse width modulation system using a modulation strategy that uses a space vector as a reference in order to achieve a desired three-level waveform (Space Vector Pulse Width Modulation). The system is specially adapted for three-phase systems that requires high-power and high-voltage and is therefore suitable for all types of renewable energy sources. As the superiority of low current harmonics and high voltage utilization, the traditional space-vector concept has been modified to be applicable for the ZSI/qZSI in [9]–[11]. The two switches' control signals of the same bridge leg are no longer complementary, even though the traditional SVM does.

The shoot-through states are inserted at the beginning or the end of active vector's switching moment to avoid the additional switching actions and losses. There are three different existing ways to distribute the shoot-through states:

1) the desired total shoot-through time interval is divided into six parts evenly distributed into six switching times [9]. The six switching times are modified, so called as ZSVM6 in this paper.

2) The divided six-part shoot-through time intervals are also fulfilled in each control cycle, but the four switching times are only modified in [10], so called as ZSVM4 here.

3) The desired total shoot through time interval is divided into four realizable parts, but two switching times are modified in [11], so called as ZSVM2. The voltage gain, voltage stress across the switch, and ac harmonics content of the three aforementioned SPWMs and the ZSVM4 are compared in [13], but it does not consider the switch current stress.

The total switching device power (SDP) was presented to evaluate both the voltage and current stresses in [18]. However, the deduced formula are not suitable for the aforementioned ZSVM*x* (*x* = 6, 4, and 2), because they have different current stress and voltage stress when compared to those in [18].

Multilevel Converters and Modulation Strategies

A DC to AC converter is defined as a inverter. The converter produces sinusoidal output waveform with respect to magnitude [V], frequency [rad/s] and phase [a,b,c] witch help from a DC-power supply. To create this specific waveform the inverter switches has to be turned ON and OFF at certain times, given by the chosen modulation strategy. As seen in Fig. 1b, the output will not be exact as a sinus wave, but the charactaristics will be the same. Fig. 1a shows a typical

ISSN: 2277-9655
Impact Factor: 1.852

three-phase two-level inverter with IGBT's (Insulated Gate Bipolar Transistor) as switching devices. The output phases are given as a,b and c. Inverters are commonly used for medium voltage applications. For high-voltage high-power applications, the inverter also serves as a control mechanism for the reactive power and voltage stabilisation. With the multilevel converter topology the output waveform can be formed with smaller voltage steps (*dv* / *dt*), which also decreases the stress on the bearings and windingisolation [7]. It obviously also gives a lower total harmonic distortion (THD) in the output because of the closer resemblance to the sinusoidal waveform.

For multilevel converters, medium voltage semiconductors devices can still be utilized for high-voltage high-power applications. Still standing is the issue with the capacitor voltage balancing problems [15]. However, still the multilevel converter dominates on the power electronic platform. The most studied and tested multilevel types are:

Cascaded H-Bridge Multilevel Converters
Flying Capacitor Multilevel Converters

Diode Clamped Multilevel Converters

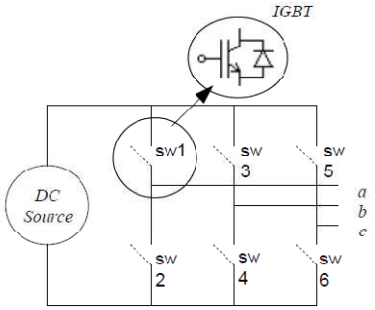

Fig.1a Three phase two level inverter

After successfully achieving the extraction of energy with help from the power converter, the next step is to connect it to the grid. This can not be done directly. The received output from the WEC has to be processed through several systems before it can match the characteristics of the grid

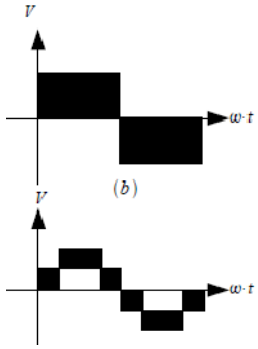

Fig 1 (b)(c), Output wave form of Line-Line and Line-Ground

Proposed Modulation strategies

Multilevel Strategies

Most of today's power systems need components making higher power operations possible. A concern for the medium voltage grid is the connection with only one semiconductor switch. This limitation became the fuel for pushing researches to develop the multilevel power converters, realizing the combination of high-power and medium-voltage.

Except for the increase of power levels, this also opened up opportunities for renewable energy sources, ie multilevel converter systems could easily be attached to it [15]. To understand this project it is necessary to go all the way back to 1981, when it all started: The Multilevel power conversion was introduced for the first time and this was only the first step in what was coming to become a foundation for today's work in power conversion.

Until then there was only some studies on PWM in general, but those were not suitable for variable drive-systems and were causing harmonic losses and torque pulsation, resulting in efficiency reduction. With the introduction of three-level converters, instead of two-level, the losses could be reduced [21]. A multilevel inverter works with the usage of several levels of DC-voltages constructing a staircase formed AC-voltage.

Capacitors, batteries and renewable energy sources can be used as the DC source [15]. When the voltage level increases the harmonics decreases. The advantage of this multilevel system is that it induces good power quality, has good electromagnetic compatibility, low switching losses and high capability [6]. There are also several methods in decreasing the switching losses even more [16]. Excepts for these advantages, the multilevel is characterized by low distortion and low *dv* / *dt* (voltage variation in time) in the output, low current distortion.

It also gives the possibility to terminate common-mode (CM) voltages (and so reducing the stress

ISSN: 2277-9655
Impact Factor: 1.852

on the bearings) [7] and is operational with both low and high switching frequencies. High switching frequency means higher efficiency [15]. Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed.

Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex [15]. This chapter will describe the three most common converters: Cascaded H-Bridge Multilevel Converters, Flying Capacitor Multilevel Converters and Diode Clamped Multilevel Converters. Also, voltage control operations will be discussed.

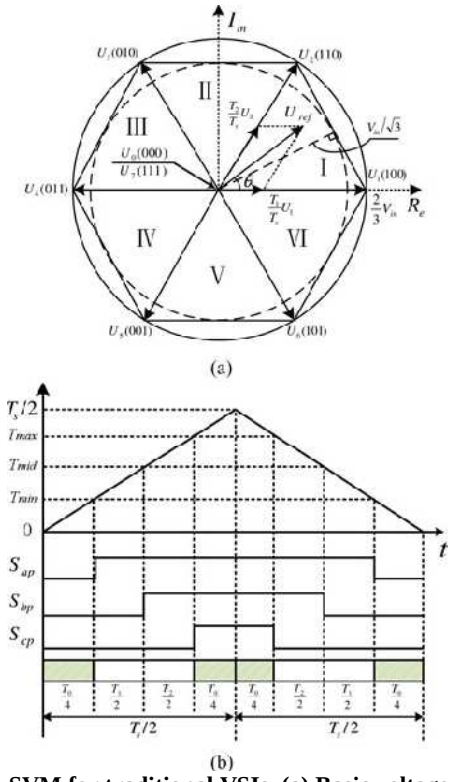

Fig. 2. SVM for traditional VSIs. (a) Basic voltage space vectors and
(b) switching time sequence.

Cascaded H-Bridge Multilevel Converters

A cascaded H-Bridge converter has several H Bridge conversion cells. These cells are formed. It consists of four switches. Each cell is also supplied with a DC-source and is series connected on the AC side. The whole figure demonstrates one phase leg for the converter. The waveform to the right is the circuits corresponding waveform. Adding VC1, VC2, VC3 and VC4 gives its 9-level step-shaped waveform [7]. Each of these levels can have +VDC, 0 and -VDC as their output through different path selections when connecting the DC-source to the AC output, thus assigning different switching patterns for the four switches.

Switch 1 and 4 switched ON gives an output of +VDC, switch 2 and 3 ON gives –VDC and all the switches ON gives a zero. The series connection between the AC outputs gives then the summation of the outputs creating this waveform. The advantages with the cascaded H-bridge multilevel converter can be seen in the formula for the calculation of the output phase voltage levels: *m*=2s1 . Given that *s* stands for the number of DC-sources needed, the number of voltage levels is more than double than for the sources. Also the series-connection of the H-bridge form lowers the manufacturing costs, because it shortens the process. The problem remaining is the fact that each H-bridge needs its own DC-source [8]. This means that it can not be connected to products that already have multiple separated DC-sources [15].

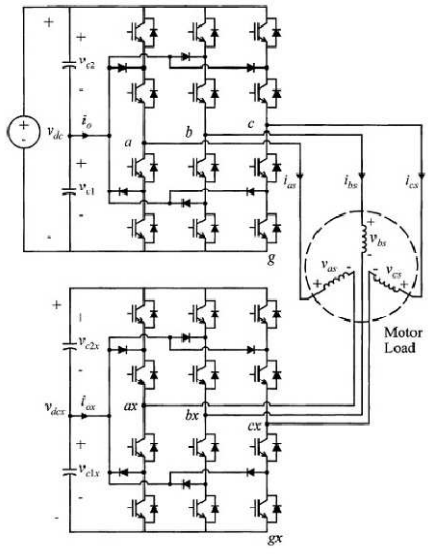

Figure 3: A two cascaded three-phase, three-level inverter

One important attribute that a multilevel converter should have is that it can be applied to as many different products as possible. There are however other types of cascaded H-bridge converters that can fit to a

ISSN: 2277-9655
Impact Factor: 1.852

wider range of product. This newer type was introduced a decade later and gave form to a converter that only needed one DC-voltage source.

In [2] and [27] this type of converter is described and realized as a two cascaded three-phase three-level inverter, as seen. Although several upgraded versions of the cascaded multilevel converter are presented, there still are problems in choosing the number of levels, with respect to the harmonic losses and costs.

It is known that higher level means less harmonics and greater output voltage, but with the advantages comes also disadvantages. It is not wisely to use as many levels as theoretically possible just to reduce the harmonics or to increase the output voltage, because more levels also means higher cost, because of more equipment.

For this particular 3/3 inverter the most eligible level is the 7-level form. Higher levels does not reduce the harmonics remarkably [4]. There are also several other methods in choosing the level best for the occasion and also methods in reducing the harmonics [3]. However, there has been studies showing that the cascaded multilevel inverter is most efficient follow voltage renewable energy sources [26].

TABLE I SIMILATION PARAMETERS

	SBC	*ZSVM6*	*ZSVM4*	*ZSVM2*	*ZSVM1*
I_{L_av}(A)	2.69	3.54	3.54	3.57	3.58
ΔI_L(A)	1.85	1.26	1.23	1.42	3.11
V_{ac}(V)	32.23	37.58	37.57	37.58	37.44

TABLE I

	SBC	*ZSVM6*	*ZSVM4*	*ZSVM2*	*ZSVM1*
I_{L_av}(A)	2.46	3.12	3.13	3.21	3.02
ΔI_L(A)	3.25	2.12	2.00	2.67	4.35
V_{ac}(V)	36.92	42.8	42.4	43.07	42.5

Its output voltage Van (one phase leg) has three states: VDC/2, 0 and -VDC/2. To get VDC/2, the two upper switches need to be ON. To get a zero, the two middle switches need to be ON and for -VDC/2 the two lower switches need to be ON. One difference between a conventional two-level inverter is the part in Fig. 3 that is called D1 and D1', referring to the two diodes. The required amount of diodes can be calculate where *m*, stands for amount of levels. So in the three-level case two diodes is needed for each phase.

The formula also shows a major increase of the number of diodes when increasing the amount of levels. A three-level inverter needs in a three-phase system 6 diodes, a four-level needs 18, a five-level 36 and at six-levels it already has reached a amount of 60 diodes. This higher level inverters may work in theory but not in practice.

The two diodes clamps the switching voltage to half of the DC-bus voltage and the difference between Va0 (for an example when S1 and S2 is on, the voltage across *a* and 0 is VDC, giving Va0 = VDC) and Van gives the voltage across one capacitor (VDC/2). It is important to add that the upper and lower switching pairs are complementary. This means that S1 and S1' or S2 and S2' never can be ON at the same time. For the five-level inverter (Fig. 7b) there are five possible voltage outputs (Van): VDC/2, VDC/4, 0, VDC/4 and VDC/2 and they operate as seen in Table 1.

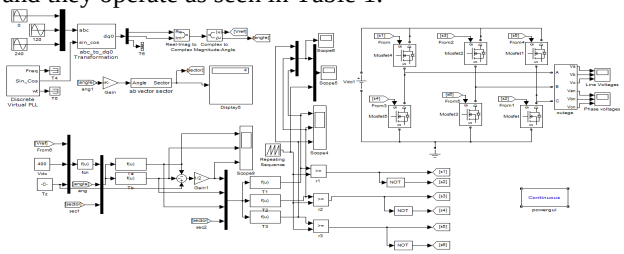

Fig.4. Modulation scheme of three phase Z source inverter

Simulation Results

Actually, this control strategy inserts shoot through in all the PWM traditional zero states during one switching period. This maintains the six active states unchanged as in the traditional carrier based PWM. The implementation of simple boost control method [7] is illustrated in Two straight lines are employed to realize the shoot through duty ratio (Do). The first one is equal to the speak value of the three-phase sinusoidal reference voltages while the other one is the negative of the first one.

When the triangular carrier waveforms is greater than the upper envelope, *Vp*, or lower than the bottom envelope, *Vn*, the circuit turns into shoot-through state. Otherwise it operates just as traditional carrier-based PWM.

Shoot-through pulses are inserted into the switching waveforms by logical OR gate. To produce switching pulses, three phase reference wave forms having peak value with modulation index (M) are compared with the same high frequency triangular signal. Comparator compares these two signals and produces pulses (when Vsin>Vtri, on and Vsin<Vtri, off). These pulses are then sent to gates of the power IGBT's through isolation and gate drive circuit.

Figure 5 shows the pulse generation of the three phase leg switches (S1, S3 and S5-positive group/upper switches and S2, S4 and S6- negative group/lower switches).This method is much uncomplicated; however,

ISSN: 2277-9655
Impact Factor: 1.852

the resulting voltage stress across the device is relatively high because sometraditional zero states are not utilized either partially or fully. This characteristic will restrict the obtainable voltage gain because of the limitation of device voltage rating. For a complete switching period, This total switching period, T0is the zero state time period and Do is the shoot-through duty ratio. In this paper, the control of ZSI is done by this control technique (SBC).

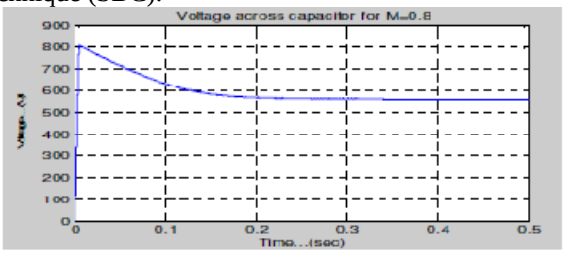

Fig. 5 Output voltage across capacitor

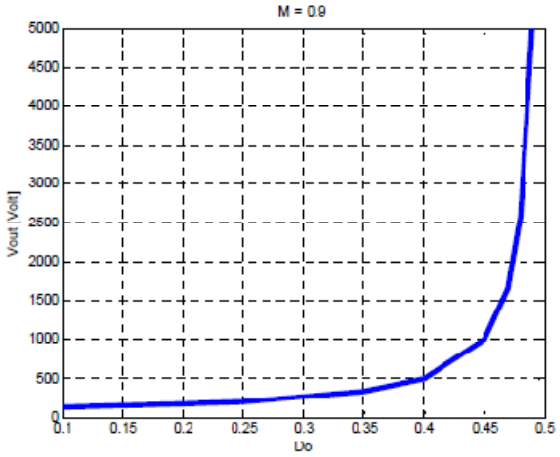

Fig.6 Output current across current

According to Table 2, the output voltage that is produced at *D0* = 0.45 and *M* = 0.55 is 1000 V. This condition actually reflects ordinary simple boost operation where *D0* + *M* = 1. The same output voltage is obtained at *D0* = 0.45 and *M* = 1, which infers that higher modulation index may be utilized. Meanwhile, Table 2 presents the output voltage and output current at fixed modulation index and variable shoot through duty ratio. It is shown from the table that the output voltage and output current rise with the increase of shoot-through duty ratio. The waveform of the output voltage and output current at *M* = 0.9 for *D0* = 0.49, *D0* = 0.45, *D0* = 0.25, and *D0* = 0.1

The plot has asymptote at *D0* = 0.5, which implies that the inverter should not be operated with *D0* very close to 0.5 since it could be burnt resulting from a very high voltage built at the output of the Simulation results for fixed duty ratio and variable modulation index are presented in Table 2 which shows the phase output voltage and phase output current at various modulation index for *Do* = 0.45 and *Do* = 0.1.

It can be seen from the table that at fixed shootthrough duty ratio, the output voltage remains constant at a specific value irrespective of the variation of the modulation index while the output current rises with the increase of the modulation index. Since the output voltages are equal, higher output current of the inverter means higher output power, which confirms the advantage of using high modulation index.

The output voltage and output current at *D0* = 0.45 for *M* = 1, *M* = 0.7, *M* = 0.55, and *M* = 0.40 are presented. The waveforms are similar to that produced with original simple boost control. inverter. After simulating and analysing the simple boost control, the maximum boost control, and the modified simple boost control, it can be concluded that:

1. The modified simple boost control generates output waveforms similar to those of ordinary simple boost control.
2. The modified simple boost control can utilize high modulation index to produce output voltage that requires high voltage gain, which may minimize voltage stress on inverter's devices.
3. Higher output voltages and output currents are obtained with higher modulation indices and or shoot-through duty ratio.
4. The shoot through duty ratio range for the modified simple boost control is lower than 0.5. These conclusions are derived from simulation results. Further analyses and investigation should be conducted to elaborate the results, which will be done in the next paper.

The aim of this paper is to present an overview of SVMs for three-phase ZSI/qZSI and compare their boost capacity, voltage stress, efficiency, etc., especially to propose the SDP for the aforementioned ZSVM*x* (*x* = 6, 4, and 2). The paper is organized as follows. The qZSI operation is illustrated in Section II, and the different ZSVMs are addressed in Section III. The total average SDP is proposed in Section IV. Simulation and experiment are carried out in Section V. Finally, Section VI concludes this study. In the following description, the qZSI is used for illustration. All PWMs can be applied to the ZSI.

Figs. 1 and 2 show the topology and equivalent circuits of the basic qZSI, respectively. As shown in Fig. 2, the qZSI has two working states. One is the shoot-through state in Fig. 2(a), where at least one bridge leg turns on. The other is the non shoot through state in Fig. 2(b), and the qZSI operates as a traditional VSI. The shoot-through state alternates with the non shoot through state by using the partial or entire

conventional zero states to boost the dc source voltage For the aforementioned SVMs of the qZSI.

The desired total shoot-through time interval is equally divided into several parts per control cycle, and each part is separately combined into the switching.

Conclusions

This paper has presented a novel transformer less active voltage quality regulator with parasitic boost circuit tomitigate long duration deep voltage sags. The proposed PB-AVQR topology is derived from the DySC circuit and the compensation performance is highly improved without increasing the cost, weight, volume, and complexity. It is a relatively cost-effective solution for deep sags with long duration time compared with the traditional DVR topology with load-side-connected shunt converter as a series transformer is no longer needed.

The working principle and circuit equations are given through theoretical analysis. Simulation and experimental results are presented to verify the feasibility and effectiveness of the proposed topology in the compensation for long duration deep voltage sags that are lower than half of its rated value. The operating efficiency of the proposed PB-AVQR system also remains at a relatively high level as the dc-link voltage adaptive control method is adopted. In a conclusion, the proposed PB-AVQR topology in this paper provides a novel solution for long duration deep voltage sags with great reliability and compensation performance

References

[1] F. Z. Peng, "Z-source inverter," *IEEE Tran. Ind Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[2] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. Power Electron. Spec. Conf.*, Rhodes, Greece, Jun. 15–19, 2008, pp. 2743–2749.

[3] Y. Li, S. Jiang, J. Cintron-Rivera, and F. Peng, "Modeling and control of quasi-Z-source inverter for distributed generation applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1532–1541, Apr. 2013.

[4] P. C. Loh, D. M. Vilathgamuwa, C. J. Gajanayake, Y. R. Lim, and C. W. Teo, "Transient modeling and analysis of pulse-width modulated Zsource inverter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 498 507, Mar. 2007.

[5] J. B. Liu, J. G. Hu, and L. Y. Xu, "Dynamic modeling and analysis of Z source converter—Derivation of ac small signalmodel and design-oriented analysis," *IEEE Tran. Power Electron.*, vol. 22, no. 5, pp. 1786–1796, Sep. 2007.

[6] W.Mo, P. C. Loh, A. Andrew, and F. Blaabjerg, "Model predictive control of Z-source neutral point clamped inverter," in *Proc IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 3838–3843.

[7] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-source inverter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 833–838, Jul. 2005.

[8] M. S. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, D. J. Adams*et al.*, "Maximum constant boost control of the Z-source inverter," in *Proc. Ind. Appl. Society*, Oct. 3–7, 2004, vol. 1, pp. 142–147

[9] Y. Liu, B. Ge, F. J. T. E. Ferreira, A.T. de Almeida, and H. Abu-Rub, "Modeling and SVM control of quasi-Z-source inverter," in *Proc. 11 th Int. Conf. Electr. Power Quality Utilisation*, Oct. 17–19, 2011, pp. 1–7.